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**Tech Insights**
**Exploring power-management design issues for advanced systems**

# MOSFETs Break Out Of The Shackles Of Wirebonding

***By Replacing Wirebonds With A Copper Strap, Power MOSFETs Finally Enter A New Era Of Electrical And Thermal Efficiency.***

**Patrick Mannion**

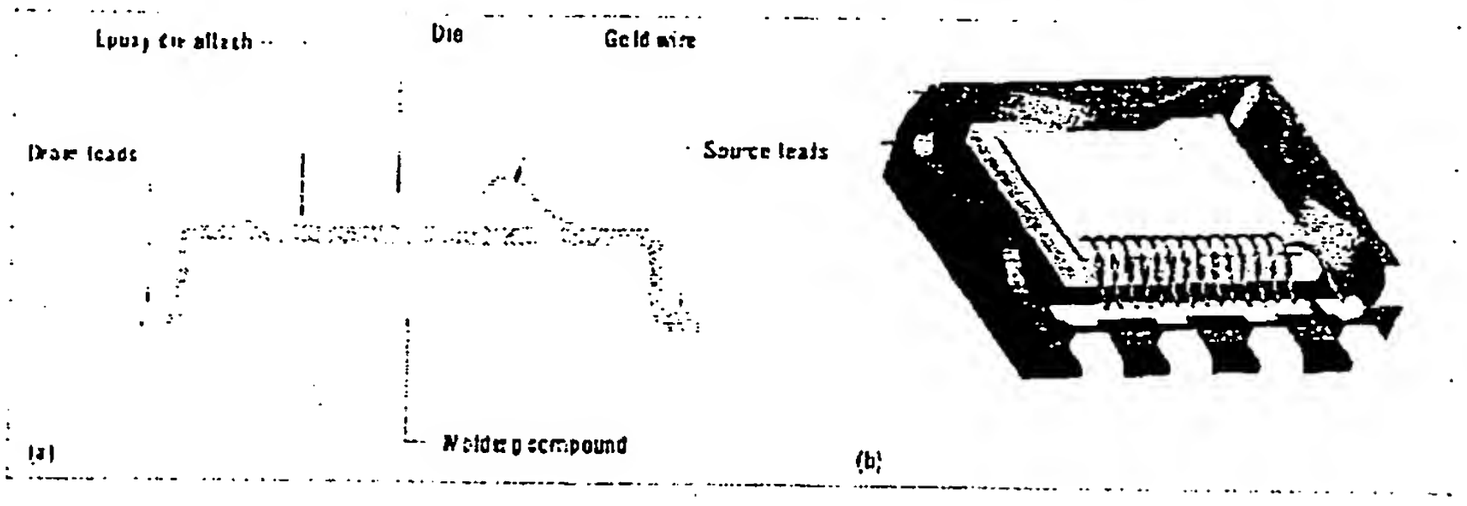
With processors, automotive electronics, and telecom board-mount applications all demanding greater power densities, thermally inefficient, high-resistance devices are wreaking havoc on system reliability. At the same time, power lost due to electrical inefficiency is draining valuable system resources. Add this to ongoing demands for lower cost, and it becomes apparent that traditional paths to efficiency nirvana are fast approaching diminishing returns. These paths, which follow the age-old practice of increasing silicon efficiency, have been so successful to date that the packaging and wirebond connections external to the die are now being recognized as the leading contributors to device inefficiency--not the die itself.

Recognizing this, International Rectifier, El Segundo, Calif., has replaced the wirebonds connecting the source to the leadframe with a solid copper strap that covers the surface of the die. This provides a highly conductive path, thermally and electrically, from the die to the leadframe and pc board. According to IR, this has resulted in a 10 to 20% reduction in thermal resistance and a 61% reduction in package contribution to electrical resistance for source connections. Called CopperStrap, the technology provides a 10 to 20% reduction in silicon temperature rise, allowing for less paralleling of MOSFETs, smaller chips and package outlines, and higher reliability.

Circumventing wwirebonding allows the CopperStrap to decrease assembly time and eliminates dreaded cratering and "purple plague" phenomena associated with wirebonds. Though not quantified as of yet, the connection methodology all but eliminates wirebond-related source inductance, a feature of

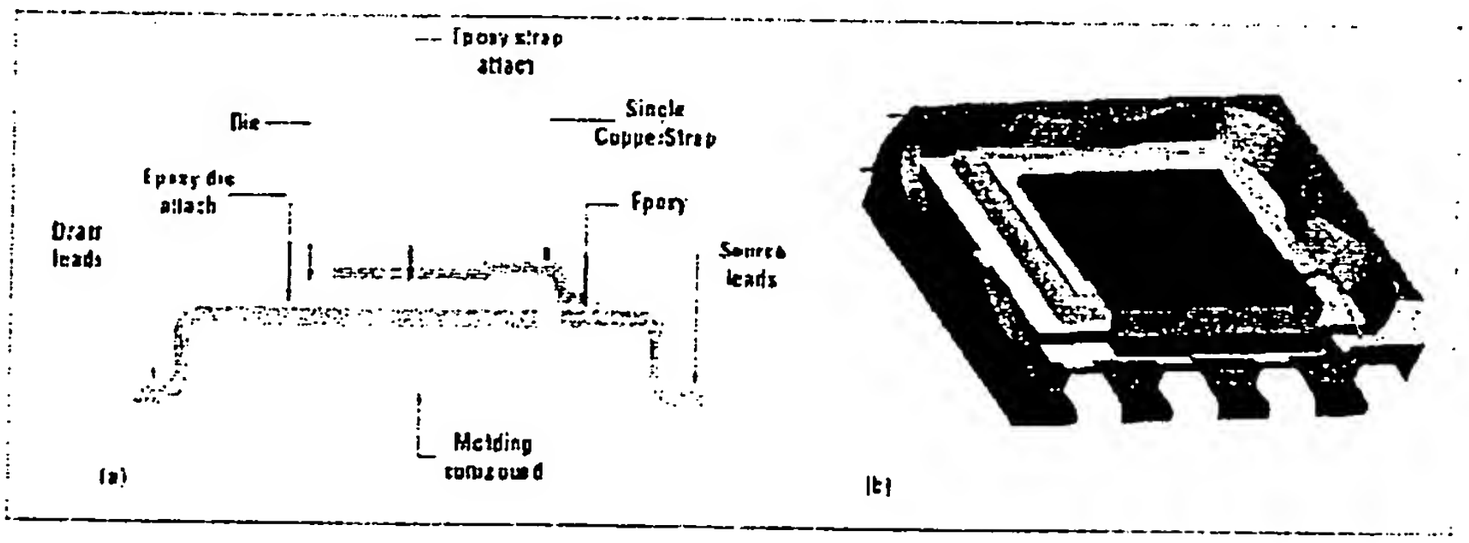
particular interest to buck-converter designers.

To date, MOSFET makers have managed to push silicon-die resistance into the single-digit milliohm range. But even this doesn't suffice. As a result, designers have been forced to opt for either a bigger, more expensive die in a larger package or for parallel arrays of less expensive devices that serve to reduce resistance, while spreading any generated heat around the board. Designs using either or both of these methods have been able to squeeze up to 10 A at 1.6 V from an input range of 10 to 21 V out of an SO-8 package. With upcoming designs looking for 15 A at 1.3 V from similarly sized or smaller packages, though, it becomes apparent that a new approach is necessary.




**1. Traditional MOSFETs use wirebonding to attach the die to the source lead and the pc board (a). The wirebonds and top-metal-sheet resistance contribute about 90% of package resistance (b). Also, gold bonds are susceptible to voids, intermetallic formations, and parasitic inductance at high frequencies.**

IR looked closely at all the elements that contribute to device resistance ***(Fig. 1a and b)***. In doing so, researchers realized that the wirebonds and top-metal-sheet resistance together contributed about 90% of the overall package resistance. The fourteen 2-mil gold wirebonds alone, already a maximum number for an SO-8 package, contributed about 1.1 m□. Replacing the wires with the CopperStrap reduced this to 0.11 m□ ***(Fig. 2a and b)***.



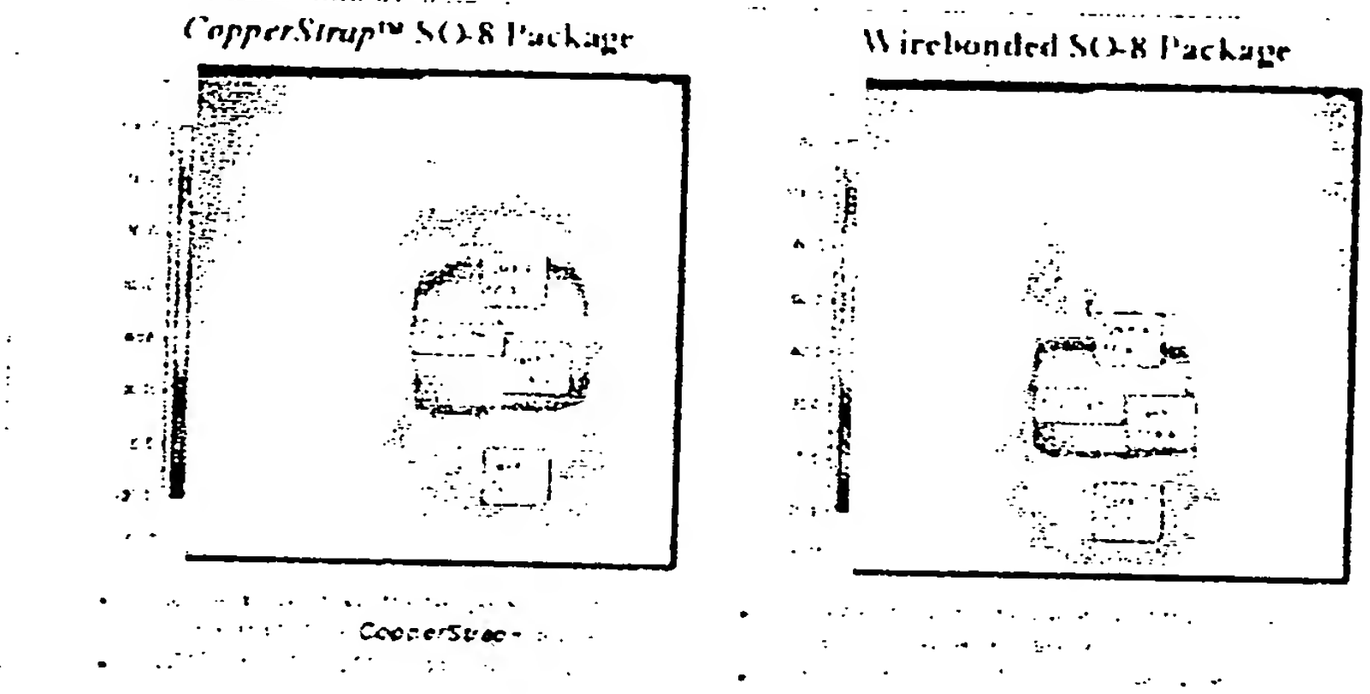

**2. Replacing the fourteen 2-mil gold wirebonds (the maximum an SO-8 package can handle) with the CopperStrap reduced the die-source resistance from 1.1 m□ to 0.11 m□ (a). The top-metal resistance of the die shrank from 1.5 m□ to about 0.7 m□ (b).**

The top-metal resistance of the die isn't normally taken into account when calculating package resistance, as it isn't considered to be part of the package. But depending on the location of the wirebonds on the top metal, 4 µm of aluminum could contribute as much as 1.5 m□. Placing the CopperStrap over most of the die's top surface provides a low-resistance parallel path, thereby reducing

the 1.5 mΩ to about 0.7 mΩ. That's a 61% reduction. If the die's top metal is much less than 4 µm, overall resistance savings could be even greater.

The implications for thermal management are even more interesting. Most of the heat from a power device in an SO-8 package is removed through a plate that forms the drain-lead connection on the back of the die. It's then conducted out to the copper in the pc board. Covering up to 70%, the top surface of the die with the copper sheet provides two thermal-dissipation avenues. The first is through the source leads to the pc board. The second takes advantage of the fact that the copper strap is routed closer to the top of the mold compound encapsulant than the traditional wirebonded solution. This allows heat to escape through radiation from the top surface of the package.

To get a better idea of how the CopperStrap theory plays out in practice, a thermograph was taken of two power MOSFETs in an SO-8 package ***(Fig. 3a and b)***. As can be seen from the image, the CopperStrap device does a much better job of conducting heat to the source leads, thereby taking it away from the die itself. This allows the device to deliver more power for a given device junction temperature.




**3. A thermograph of two power MOSFETs in an SO-8, one with the CopperStrap (a) and one with wirebonding (b), shows how the CopperStrap device conducts more heat to the source leads, taking it away from the die. This allows the device to deliver more power for a given device junction temperature.**

The CopperStrap's thermal capabilities can be put to maximum use in applications such as synchronous buck converters. Here, the low-side MOSFET's source connection is at ground potential. By increasing the thickness and area of the copper ground plane on the pc board, more heat can be pulled out of the die through the source pins.

CopperStrap has an extra advantage in buck converters. Its reduced source inductance is a result of wire elimination. But the degree to which performance has been improved hasn't been quantified yet.

On the reliability end, getting rid of the gold wire eliminates two major problems. First is wirebond cratering. It occurs when silicon fractures as a result of unoptimized wirebond parameters--the bonding force, as well as the intensity and duration of ultrasonic power. Cratering can't be detected reliably at final test. Therefore, it usually appears during reliability testing or in the field.

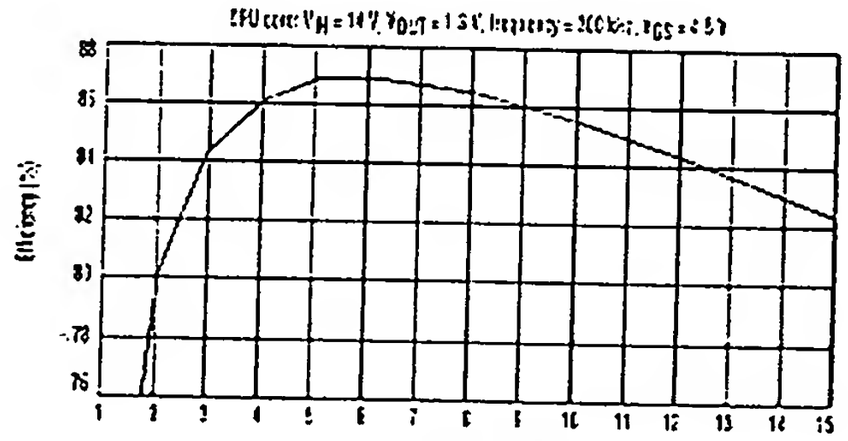
CopperStrap also puts an end to "purple plague." When gold is combined with an aluminum top metal, there's a risk of intermetallic formations. When exposed to high temperatures and/or small levels of

contaminants, the formations can be accelerated and can result in Kirkendall voids. These act in series with overall package resistance and can even result in complete open conditions. Purple plague can't be detected at final test, either. And once present, it can be very difficult to contain or control.

Other materials issues come into play. While copper is compatible with silver-filled epoxy and aluminum top metal, properties of the molding compound and silver-filled epoxy must be selected to optimize thermal, mechanical, and moisture resistance. Also,copper's expansion rate is different from that of gold wires. This has to be taken into account, especially when exposed to high solder-reflow temperatures and temperature cycling. The shape and features of the strap play a key role in how well stresses are distributed under these conditions.

| KEY DEVICE PARAMETERS | | |
|---|---|---|
| **Parameter** | **IRF7809** | **IRF7811** |
| $V_{DS}$ | 30 V | 30 V |
| $R_{DS}(ON)TYP$ | 6mΩ | 9mΩ |
| $Q_{G\ (TYP)}$ | 63 nC | 18.2 nC |
| $Q_{SWITCH\ (TYP)}$ | 16.2 nC | 5.8 nC |
| $R_{TH\ J\ LEAD\ (MAX)}$ | 20°C/W | 20°C/W |
| $R_{TH\ J\ AMB\ (MAX)}$ | 35°C/W | 35°C/W |
| Qswitch = $Q_{GS}2 + Q_{GD}$, where $Q_{GS}2$ = post gate-source threshold charge. | | |

CopperStrap is available in a dual chipset version: the high-side IRF7809, which uses PlanarFET technology, and the low-side TrenchFET-based IRF7809. Key performance specifications for these devices are shown **in the table**. The combination's ability to achieve efficiencies of up to 87% at 14 $V_{IN}$/1.3 $V_{OUT}$/6 A also is shown ***(Fig. 4)***. Efficiency falls off to about 83% at 15 A.



**4. To date, the CopperStrap is capable of achieving efficiencies of up to 87% at 6 A. The efficiency falls off to about 83% at 15 A.**

Cost per device is an extremely important facet of any product change or modification. In this case, there's no cost barrier, as the same manufacturing techniques and tooling can be used with minor adjustments. The only additional operation is the copper-strap placement, which can actually be incorporated into the existing die-attach operation.

## Price And Availability

*The IRF7809 and IRF7811 will be available in June as a chipset for $1.25 each per pair in 100,000-unit*

*quantities.*

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